Amendments to the Specification

Please add the following paragraph between the title and the first line of text as follows:

This is a Division of Application No. 09/424,718 filed February 4, 2000. The entire disclosure of the prior application is hereby incorporated by reference herein in its entirety.

Please replace the paragraph beginning on page 12, line 3, with the following rewritten paragraph:

In this case, the trace information output section 1416 outputs trace information for implementing a real-time trace, to four dedicated terminals. More specifically, it outputs instruction execution status information (DST[2:0]) of the CPU to three terminals at each clock signal, to function as a status information output means. In addition, if PC absolute branch execution occurs, it outputs the PC value (DPCO) of the branch destination serially from the single terminal during the subsequent 27 clock cycles.

Please replace the paragraph beginning on page 18, line 5, with the following rewritten paragraph:

The clock generation section 30 generates the various clock signals used within the microcomputer 10. The clock generation section 30 also supplies a clock signal to an external debugging tool 2060 via the BCLK.

Please replace the paragraph beginning on page 21, line 27, with the following rewritten paragraph:

The CPU 12 sends a pre-fetch request signal (CPU_IR_REQ) to the BCU 26 through the line 170 (412 in Fig. 8) and sends the instruction address (IA) to be fetched to the BCU 26 through the line 178 (418 in Fig. 8). On receiving the CPU_IR_REQ signal 412, the BCUBUC 26 sends a signal indicating that that signal has been received (CPU_IR_ACK)

through the line 172 to the CPU 12 (414 in Fig. 8). It also sends the instruction code (IR_CODE) that has been read from that instruction address (IA) through the line 176 to the CPU (420 in Fig. 8) and sends a signal indicating that the instruction code has been sent (CPU_IR_VLD) through the line 174 to the CPU (416 in Fig. 8).

Please replace the paragraph beginning on page 24, line 13, with the following rewritten paragraph:

Illustrations of the relationship between a branch instruction and a reset are shown in Figs. 9A and 9B. Fig. 9A shows the FIFO state before a branch instruction is executed and Fig. 9B shows the FIFO state after a reset. If there is a write pointer at 380, a branch instruction has been executed. If that occurs, comparison results 382 ~~(shaded portion)~~ with the pre-fetched instruction will become comparison results for a non-executed instruction.

Please replace the paragraph beginning on page 26, line 26, with the following rewritten paragraph:

An RS232C interface 114 and a parallel interface 116 provide interfaces with the host system 66 of Fig. 6, and debugging commands from the host system 66 are input to the CPU 90 through these interfaces. A clock generation section 119~~118~~ is designed to generate clock signals, such as the clock that causes the CPU 90 to operate.

Please replace the paragraph beginning on page 27, line 14, with the following rewritten paragraph:

When the microcomputer is in user mode (when a user program is executing), the line 122 is selected so that the output of the address incrementer 100 is input to the address terminal of the trace memory 24 through the selector 102. In addition, when the microcomputer is in user mode, the line 126 is selected so that DST[2:0] and DPCO are input to the data terminal of the trace memory 24~~104~~ through the selector 106. In this case, a start

address is set initially by the CPU 90 in the address incrementer 100, using the data bus 118 and the address bus 120, as shown in Fig. 11A. A DST[2] line that specifies the trace range is also connected to a start/stop (ST/SP) terminal of the address incrementer 100. When a first pulse 390 is input to the DST[2] line, the address incrementation of the address incrementer 100 starts. When a second pulse 392 is input to the DST[2] line, the address incrementation of the address incrementer 100 stops and the trace operation halts. In this manner, data (DST[2:0] and DPCO) for the desired trace range can be stored within the trace memory 24.

Please replace the paragraph beginning on page 28, line 17, with the following rewritten paragraph:

56. Electronic Equipment

The description now turns to electronic equipment comprising the microcomputer of the present embodiment.